**ECE 3663**

**Design Review 1 – Simulation Results**

**Group: ADD**

**3/13/2012**

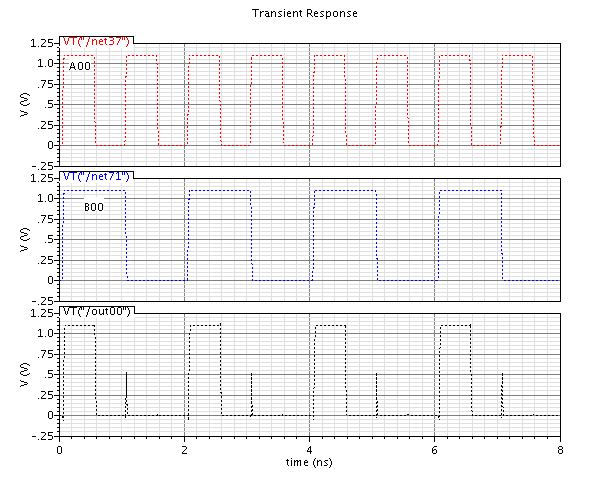
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1. AND simulation results – transient signal graph:



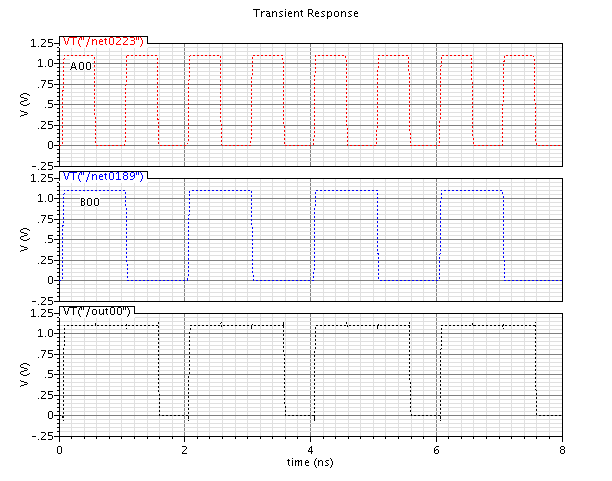
Above is the transient response for the one-bit location in the 16-bit AND gate with input A00, B00, and output out00.

A00 has an input pulse signal with period = n, delay time = 0, rising/fall time = 0.1n and width = 0.4n.

B00 has an input pulse signal with period = 2n, delay time = 0, rising/fall time = 0.1n and width = 0.9n.

The resulting output signal demonstrates that the AND gate functions correctly in all lines in the truth table:

1. A=0, B=0: in time of 1.5n to 2n, output = 0;
2. A=0, B=1: in time of 0.5n to 1n, output = 0;
3. A=1, B=0: in time of 1n to 1.5n, output = 0;
4. A=1, B=1: in time of 0n to 0.5n, output = 1.
5. OR simulation results – transient signal graph:



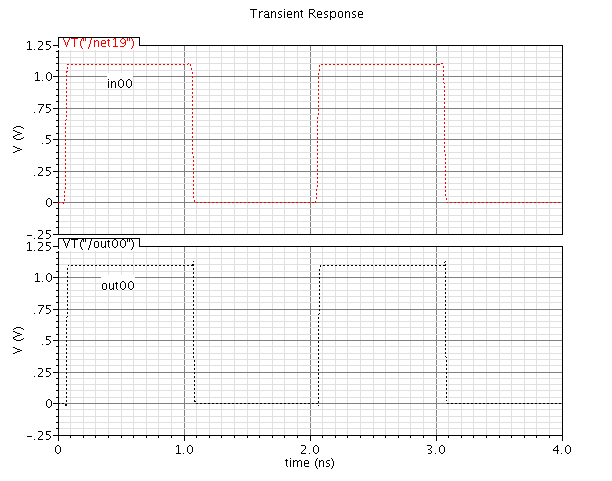
Above is the transient response for the one-bit location in the 16-bit OR gate with input A00, B00, and output out00.

A00 has an input pulse signal with period = n, delay time = 0, rising/fall time = 0.1n and width = 0.4n.

B00 has an input pulse signal with period = 2n, delay time = 0, rising/fall time = 0.1n and width = 0.9n.

The resulting output signal demonstrates that the OR gate functions correctly in all lines in the truth table:

1. A=0, B=0: in time of 1.5n to 2n, output = 0;
2. A=0, B=1: in time of 0.5n to 1n, output = 1;
3. A=1, B=0: in time of 1n to 1.5n, output = 1;
4. A=1, B=1: in time of 0n to 0.5n, output = 1.
5. PASS simulation results – transient signal graph:

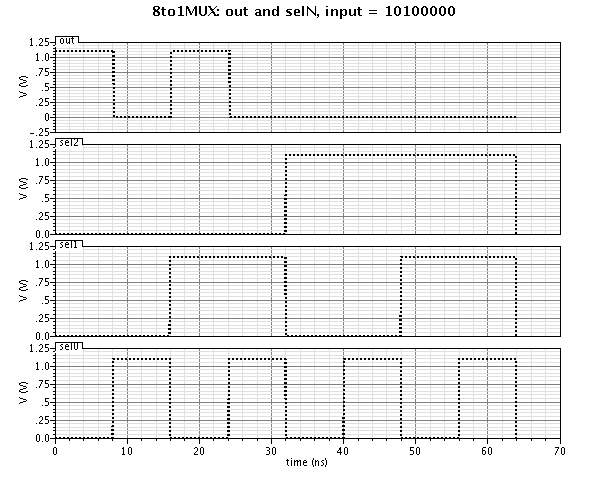


Above is the transient response for the one-bit location in the 16-bit PASS with input in00 and output out00.

in00 has an input pulse signal with period = n, delay time = 0, rising/fall time = 0.1n and width = 0.4n.

The resulting output signal demonstrates that the PASS functions correctly in all lines in the truth table:

1. in00=0: in times of 0.5n to 1n, output=0;
2. in00=1: in times of 0n to 0.5n, output=1.
3. 8-1 MUX simulation results – transient signal graph:

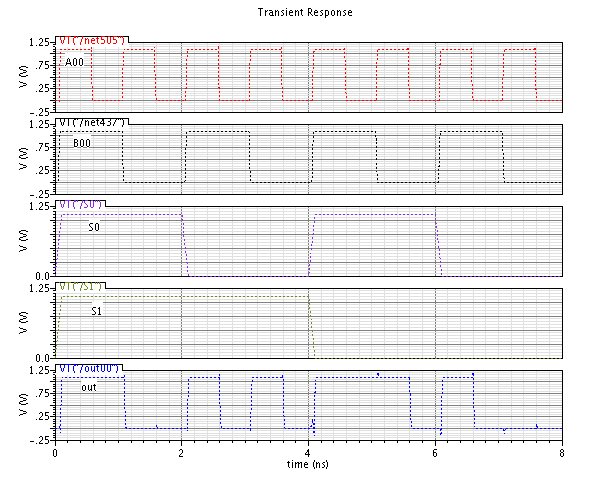


Above is the transient response for the 8-1 MUX with selection lines sel2, sel1, sel0, input = 10100000, and output out.

Sel2 has an input pulse signal with period = 4n, sel1 has an input pulse signal with period = 2n, and sel0 has an input pulse signal with period = n.

The resulting output signal demonstrates that the 8-1 MUX functions correctly in all lines in the truth table:

1. Sel2=0, sel1=0, sel0=0: in time of 0n to 0.5n, out=1 (1st bit of input);
2. Sel2=0, sel1=0, sel0=1: in time of 0.5n to 1n, out=0 (2nd bit of input);
3. Sel2=0, sel1=1, sel0=0: in time of 1n to 1.5n, out=1 (3rd bit of input);
4. Sel2=0, sel1=1, sel0=1: in time of 1.5n to 2n, out=0 (4th bit of input);
5. Sel2=1, sel1=0, sel0=0: in time of 2n to 2.5n, out=0 (5th bit of input);
6. Sel2=1, sel1=0, sel0=1: in time of 2.5n to 3n, out=0 (6th bit of input);
7. Sel2=1, sel1=1, sel0=0: in time of 3n to 3.5n, out=0 (7th bit of input);
8. Sel2=1, sel1=1, sel0=1: in time of 3.5n to 4n, out=0 (8th bit of input).
9. Bonus simulation results – transient signal graph:



Above is the transient response for the bonus part: using a 4:1 mux with selection lines S0 and S1 to select the output of one of the four gates: AND, OR, PASS A and PASS B. The graph is for one bit location with input A00 and B00.

S1 has an input pulse signal with period = 8n, S0 has an input pulse signal with period = 4n, B00 has an input pulse signal with period = 2n, and A00 has an input pulse signal with period = n.

The resulting output signal demonstrates that the 4:1 MUX functions correctly in all lines in the truth table:

1. S1=0, S0=0: in time of 6n to 8n, output = AND;
2. S1=0, S0=1: in time of 4n to 6n, output = OR;
3. S1=1, S0=0: in time of 2n to 4n, output = PASS A;
4. S1=1, S0=1: in time of 0n to 2n, output = PASS B.